Docket No. 279690US2PCT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Masayuki YOSHIDA, et al.

SERIAL NO: 10/553,517 GAU:

FILED: October 14, 2005 EXAMINER:

FOR: METHOD OF FORMING SHEET HAVING FOREIGN MATERIAL PORTIONS USED FOR FORMING MULTI-LAYER WIRING BOARD AND SHEET HAVING FOREIGN PORTIONS

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

■ Attached is a list of applicant's pending application(s), published application(s) or issued patent(s) which may be related to the present application. In accordance with the waiver of 37 CFR 1.98 dated September 21, 2004, copies of the cited pending applications are not provided. Cited published and/or issued patents, if any, are listed on the attached PTO form 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

ATTY DOCKET NO.	SERIAL NO.
279690US2PCT	10/553,517
APPLICANT	
Masayuki YOSHIDA, et al.	
FILING DATE	GROUP
October 14, 2005	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2005 0194084	09/08/05	YOSHIDA et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AB	2000-40633	02/08/00	JP (equivalent of US 2003/0038372 & US 6555913)		NO
	AC	11-186097	07/09/99	JP (equivalent of EP 0938107, US 2001/0020754 & US 6413456)		NO
	AD	2001-110662	04/20/01	JP		NO
	AE	59-32115	02/21/84	JP		NO
	AF	2001-267167	09/28/01	JP		NO
	AG	9-199663	07/31/97	JP (equivalent of US 5722162 & US 5930890)		NO
	AH	2000-182870	06/30/00	JP		NO
	AI	2001-085264	03/30/01	JP (with English abstract)		NO
	AJ	2001-110662	04/20/01	JP (with English abstract)		NO
	AK	2001-076959	03/23/01	JP (with English abstract)		NO
	AL	2000-331858	11/30/00	JP (with English abstract)		NO
	AM	2000-331865	11/30/00	JP (with English abstract)		NO
	AN	2001-111223	04/20/01	JP (with English abstract)		NO
	AO	2000-183530	06/30/00	JP (with English abstract)		NO
	AP	10-012455	01/16/98	JP (with English abstract)		NO
	AQ	06-059117	03/04/94	JP (with English abstract)		NO
	AR	06-204665	07/22/94	JP (with English abstract)		NO
	AS	2000-164457	06/16/00	JP (with English abstract)		NO
	AT	6-36472	05/11/94	JP (with English abstract)		NO
	AU	50-2059	01/23/75	JP (equivalent of GB 1 262 245)		NO
	AV	51-118390	10/18/76	JP (with English abstract)		NO
	AW	58-93298	06/02/83	JP		NO
	AX	3-7157	01/31/91	JP (equivalent of US 4 673 773)		NO
	AY	61-90496	05/08/86	JP (equivalent of US 4 659 587)		NO
	AZ	5-39119	06/14/93	JP		NO
	AAA	61-127196	06/14/86	JP		NO
	AAB	4-38158	06/23/92	JP		NO
	AAC	63-43396	02/24/88	JP		NO
	AAD	3-1830	01/11/91	JP (equivalent of US 4 908 689 & EP 0 246 447)		NO
	AAE	63-244797	10/12/88	JP		NO
	AAF	07-211571	08/11/95	JP (English abstract only)		NO

Examiner | Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

U.S. PCT Application Serial No: 10/553,517
Filed: October 14, 2005
Masayuki YOSHIDA, et al.
Docket No. 279690US2PCT

STATEMENT OF RELEVANCY

1) References AB-AH have been cited in the International Search Report. A copy of these references is being submitted herewith.

2) Reference AAF has been cited in the corresponding International Preliminary Examination Report. A copy of this reference is being submitted herewith.

3) References AI-AP are discussed in the specification. A copy of these references is being submitted herewith.

4) References AQ-AAE are additional prior art known to Applicant. A copy of these references is being submitted herewith.

AW JP 58-93298

Describes a lower layer wiring pattern that is produced by forming a wiring conductor layer on a substrate, and then forming a resist layer thereon. Next the resist layer is partly removed to form through-holes and an interlayer insulation film constituting multi-layer wiring is formed by using a polyimide based resin. A resist film is then formed on the insulation layer, connecting through-holes are formed by partly removing the resist film, the insulation layer is baked and upper layer wiring is formed on the resulting insulation layer.

AZ JP 5-39119 and AAA JP 61-127196

A method is described which uses the above insulation layer etching method to form wiring patterns of materials such as copper or chromium on the surface of an insulation layer by plating, sputtering, or evaporation and, at the same time, makes the via hole portions conductive in order to electrically connect with a lower layer conductor pattern.

The steps involved in the plating pillar method are shown in Figure 5 (a) to (h). In this method, a metal film for lower layer wiring circuit 103 is deposited on a substrate 101 blanket coated with polyimide resin using film forming techniques such as sputtering. A lower layer wiring circuit 103 is formed by photosensitive resist coating, pattern exposure, developing, resist removing, and etching (Figure 5 (a)).

Then photosensitive resist 104 is blanket coated on the lower layer wiring circuit 103 (Figure 5 (b)), and selectively removed after pattern exposure and development to form a resist hole 105 (Figure 5(c)). A plating pillar 106 is formed in true resist hole 105 by, for example,

AZ JP 5-39119 and AAA JP 61-127196 cont.

electroplating (Figure 5(d)), and then the resist 104 is removed by use of predetermined solvent (Figure 5 (e)). Next, polyimide 107 is applied thereon (Figure 5 (f)), and the surface of the polyimide is smoothed by polishing to expose the top of the plating pillar 106 (Figure 5 (g)). The an upper layer wiring circuit 108 is formed thereon by a film forming technique such as sputtering (Figure 5 (h)). Multi layer wiring can be formed by repetition of these processes.

AAB JP 4-38158

Describes a process in which a wiring pattern of copper is formed on a ceramic substrate a lower layer of wiring and then a photoresist pattern is formed thereon by use of ordinary photolithographic technique. Next, the lower wiring layer surface exposed through a photoresist hole is electroplated to form a plating pillar. The entire exposed surface of the above plating pillar and the substrate is coated with polyimide resin, and a specified pressure is applied from the surface of the insulation layer toward the substrate in order to make the insulation layer surface layer. Then an upper wiring layer is deposited in a specified position on the insulation layer surface to form wiring.

AAC JP 63-43396

Describes a process multilayer wiring is produced by forming a lower layer of wiring on the entire surface of a multi-layer wiring alumina substrate, and, after a positive type dry film is pressure bonded, a resist pattern is formed through exposure and development. Next a plating pillar is produced in the formed via hole by electroplating, and the plating resist pattern is removed by solvent.

An insulation layer is applied thereon, the surface of the insulation layer is ground to expose the top of the plating pillar, another insulation layer is applied thereon, a resist hole of a desired diameter is formed in this insulation layer, copper is sputter coated in the resist hole and on the surface of the above insulation layer, and the necessary circuit pattern is formed by etching to obtain multi-layer wiring.

AAE JP 63-244797

Describes a process in which a positive-type dry film is laminated onto an aluminum substrate (which has a lower-layer wiring pattern formed thereon) to form a resist pattern. Resist holes are formed by exposure and development and then the resist holes are plated with copper sulphate to form a plating pillar, before removing the remaining resist with acetone. The pillar is then coated with a polyimide insulation layer, the surface of the insulation layer is polished to expose the head of the pillar, and a copper layer is deposited on

AAE JP 63-244797 cont.

the surface of the insulation layer and the head of the plating pillar with sputtering apparatus to form a desired wiring pattern.

	Docket No.: 279690US2PCT	Serial No.: 10/553,517
LIST OF RELATED CASES CITED BY APPLICANT UNDER 37 CFR 1.56	Inventor: Masayuki YOSHIDA, et al.	
	Filing Date: October 14, 2005	Group:

LIST OF RELATED CASES

Examiner Initial	Docket No.	Serial or Patent Number	Filing or Issue Date	Patent App. Publication No.	Inventor or Applicant
	267074US2	11/068,781	03/02/05	2005-0194084	YOSHIDA et al.
	279690US2 PCT*	10/553,517	10/14/05		YOSHIDA et al.

Examiner

Date Considered

*Present Application; listed for information

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